

JCC 79 V.8 PTO  
09/910753

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Class	Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

## U.S. **UTILITY** Patent Application

 <b>O.I.P.E.</b>	<b>PATENT DATE</b>
<b>SCANNED</b> <u>AC<sup>3</sup></u> <b>Q.A.</b> <u>09/3</u>	

APPLICATION NO. 09/910753	CONT/PRIOR	CLASS 257 428	SUBCLASS 378 734	ART UNIT 281 0826	EXAMINER Forde
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APPENDIX

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TIME

Structure and method for fabricating configurable transistor devices utilizing the formation of a compliant substrate from materials used to form the same.

PTO-2040  
12/99

## **ISSUING CLASSIFICATION**

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	

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